

# **BSD - BOUNDARY-SCAN DIAGNOSTICS**

### Clear interpretation of JTAG test results



- Post processor operates on existing results
- No test repeat needed
- For interconnects, memory clusters & logic clusters
- Output format to Visualizer for graphic fault display
- Pin-point multiple fault-types to pin-level
- Floating license can be shared across run-time systems

Screenshot showing BSD text output and subsequent display in Visualizer layout & schematic.

### Introduction

BSD is an optional, advanced software module that works as a post-processor for the results data derived from a JTAG Technologies test execution. Applying BSD to test results gives test engineers, rework technicians and repair depots precise indicators for PCB and/ or system faults that can be displayed as a text output or optionally viewed graphically in JTAG Technologies' Visualizer viewers. These indicators are expressed as:-

- · Bridging faults (circuit network shorts)
- $\cdot$  Nets stuck-at 1 faults (nets shorted to power/Vcc)
- $\cdot$  Nets stuck-at 0 faults (nets shorted to ground/0v)
- · Pin stuck-at faults (open pins)
- $\cdot$  Twist faults (network terminals swapped or crossed)
- · IEEE std. 1149.6 LVDS network faults various.

#### Test Application Types

In all fault cases, precise location data is offered that includes device references and device pin numbers. JTAG Technologies applications that are supported by BSD include:

#### a) Interconnection Testing

For most designs the majority of the test coverage comes from the execution of this test that is used to detect

faults on the connections between boundary-scan (IEEE 1149.x) parts. As standard the results of the interconnection test are displayed as a Truth Table Report (TTR) and while useful it is not always clear what faults have occurred, especially in the case of multiple simultaneous faults. By applying the BSD tool, results are thoroughly processed and verbose 'English Language' fault reports are produced – see example screen 1.

b) Memory Interconnection Testing (inc. Flash parts) Many designs feature memory 'clusters' or banks that connect to a boundary-scan compliant part. In these cases JTAG ProVision can be used to automatically generate a memory cluster test. Interpreting the TTR results of a memory test can be difficult, especially on address line faults that can only be derived from incorrect data bus returned values. In these cases BSD offers an extremely valuable function that pin-points the faults precisely.

#### c) Logic Cluster Testing

Using BSD with logic clusters requires the user to define a fault dictionary file (.dic) using Mentor Graphics' Quick-Fault syntax. Full instructions on how to construct a fault dictionary file to detect stuck-at faults are included in the BSD manual that accompanies this option.

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### **BSD** report output options

When using BSD in ProVision the standard text output will be visible in the BSD window, however, further output options (see below) are available if BSD is launched from the command line or via one of JTAG Technologies PIP (Production Integration Package) options for Lab-VIEW, LabWindows, C, VB, TestStand or .NET. Note that the license for the PIP-specific BSD function is provided by the BSD license feature and is not a standard part of any PIP.

· DIA file – default standard text output file as displayed within ProVision and AEX/VIP Manager (Classic tools)

• DRC/DRC2 file – diagnostic record type format. Original DRC format can be used for single PCB test arrangements while DRC2 format accommodates test results from projects featuring multiple boards. The results in DRC/DRC2 files are presented in a tabulated format for easier import into a spreadsheet or process control tools.

• IMSG file – information message, a text format that is always produced by BSD. IMSG files are imports to JTAG Technologies Visualizer graphical design viewers. Using BSD in conjunction with Visualizer allows fault nets and pins to be highlighted within layout or schematic diagrams

 $\cdot$  HTML file – results output format for easier viewing within a web-browser for example.

#### BSD Output Options HTML

erd	Net	Device	PinType	PinNr	PinId												
Single 2156_1	net P3_16	04	BScan InOut	F17	P3_16		nterconnect	test.drc2							(		
Single	net	34	Incut	9	-		A	В	С	D	E	F	G	н	1	J	
2156 1	P4 9	04	BScan InOut	H17	P4 9	1	DESIGN:	t2156									
		34	InOut	2	-	2	TEST:	Interconnect	test								
						3	VERSION	2									
						4											
						5	Test	Interconnect test	Start								
						7	NetCAO	ROADD	20100 1	NET	02.46		-				
						0	Dielefe	BOARD	2100 1	NET	P3_10	10	14	DIM		4	
						0	Dislafa	BOARD	20100 1	NET	P3 10	10	114	DIN	E47	4	
						3	Pininio	BOARD	Jr2 100_1	NET	PJ_10	10	0.0	PIN	P II		
						11	Bridge	BOARD	jt2156_1	NET	P3_16	-	BOARD	jt2156_1	NET	P4_9	
						12	PinInfo	BOARD	jt2156_1	NET	P3_16	IC	J4	PIN		4	
						13	PinInfo	BOARD	12156 1	NET	P3 16	IC	U4	PIN	F17		
						14	PinInfo	BOARD	jt2156_1	NET	P4 9	IC	J4	PIN		2	
						15	PinInfo	BOARD	12156_1	NET	P4 9	IC	U4	PIN	H17		
						16	Test	Interconnect test	Failed								
						17											
						12	To Tank						1.1			-	
						L.L.	I III	terconnect test/					1 ·			House,	

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